AFRL-OSR-VA-TR-2013-0531

BIOLOGY OF MEMRISTOR MINDS

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07/01/2013
Final Report

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YYYY)*	**2. REPORT TYPE**	**3. DATES COVERED** *(From - To)*
21-06-2013	Final Report	June 15, 2010-June 14, 2013

4. TITLE AND SUBTITLE

Biology of Memristor Minds

5a. CONTRACT NUMBER

5b. GRANT NUMBER

FA 9550-10-1-0290

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)

Leon O Chua

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

University of California, Berkeley
CA 94720

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)

Air Force Research Lab
Arlington, VA 22203

10. SPONSOR/MONITOR'S ACRONYM(S)

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION / AVAILABILITY STATEMENT

Public Release

13. SUPPLEMENTARY NOTES

14. ABSTRACT

During the past 3 years, we have exploited the memristor's enabling potentials for designing intelligent machines with "learning and adaptive" capabilities. We have conducted an in-depth study of the nonlinear dynamics of several ion-channels which underpins the biological basis of life itself, where voltage-gated ion channels, with their complex biochemical synaptic dynamics, are memristors.

We have discovered that the Hodgkin-Huxley axon is made of memristors, in addition to conventional circuit elements. In particular, we have proved that the potassium voltage-gated ion channel is a first-order voltage -controlled memristor, and that the sodium voltage-gated ion channel is a second-order voltage-controlled memristor. We have derived the DC V-I curves of the potassium and sodium ion channels, as well as that of the Hodgkin-Huxley Axon. The most significant result of our 3-year research is our derivation of the "memristor-based" Hodgkin-Huxley Axon circuit model, which along with our "principle of local activity" and its gem, the "edge of chaos", allow us to resolve 3 fundamental unsolved problems from Neurobiology, including the precise nonlinear dynamical mechanism which gives rise to the "action potential".

15. SUBJECT TERMS

memristor, Hodgkin-Huxley axon, potassium voltage-gated ion channel, first-order voltage -controlled memristor, sodium voltage

16. SECURITY CLASSIFICATION OF:			**17. LIMITATION OF ABSTRACT**	**18. NUMBER OF PAGES**	**19a. NAME OF RESPONSIBLE PERSON**
					Leon O Chua
a. REPORT	**b. ABSTRACT**	**c. THIS PAGE**	SAR	17	**19b. TELEPHONE NUMBER** *(include area code)*
					510-848-7652

FINAL REPORT

June 15, 2010-June 14, 2013

Biology of Memristor Minds

(FA 9550-10-1-0209)

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INTRODUCTION

During the grant period June 15, 2010-June 14, 2013, we have focused our research on the following fundamental aspects of biological Memristors.

1. *Memristor synaptic memories*
2. *Memristor chaotic dynamics*
3. *Memristor autoassociative memories*
4. *Memristor cellular Automata*

An in-depth understanding of the above areas is essential for endowing *artificial intelligence to memristor brain-like computers*, we have made major advances in each of these 4 inter-related areas. Particularly, we have focused our research on deriving the memristive-based Hodgkin-Huxley axon model, along with its small-signal circuit model, where all circuit elements are defined by explicit formulas, therefore allowing, for the first time, a comprehensive circuit analysis of the small-signal dynamics of the Hodgkin Huxley axon, by examining the zeros and the frequency response of the associated admittance function, about each applied external DC

current. We were also able, for the first time, to derive the exact Real Part Re[Y(iω)] and the Imaginary part Im[Y(iω)], in analytic form. These in depth analysis allows us to carry out an in depth nonlinear analysis of the bifurcation phenomena in the Hodgkin-Huxley axon. A rather surprising major result from this research is that the Hodgkin-Huxley axon is poised near the "edge of chaos", an exciting and important area.

We have also simultaneously carried out research on inventing efficient circuits for tuning the memristor synaptic weights essential for learning and adaptation. To understand the highly complex nonlinear dynamics and bifurcation phenomena in memristive circuits, we have discovered an important class of memristive circuits which can be described by a Hamiltonian equation. This is a fundamental discovery at the foundation of memristive neural circuits.

SUMMARY OF RESEARCH

Following is a list of all papers citing AFOSR support which are published during the period June 15, 2010 to June 14, 2013.

1. L. Chua, **"Resistance switching memories are memristors,"** *Applied Physics A,* vol. 102, no. 4, pp. 765-783, Apr. 2011.

2. J. M. Ginoux, C. Letellier and L. O. Chua, **"Topological analysis of chaotic solution of a three-element memristive circuit,"** *International journal of Bifurcation and Chaos,* vol. 20, no. 11, pp. 3819-3827, Nov. 2010.

3. M. Itoh and L. Chua, **"Auto associative memory cellular neural networks,"** *International journal of Bifurcation and Chaos,* vol. 20, no. 10, pp. 3225-3266, Oct. 2010.

4. L. Chua and G. Pazienza, **"A nonlinear dynamics perspective of Wolfram's new kind of science. Part XIV: More Bernoulli σ_T -Shift Rules,"** *International Journal of Bifurcation and Chaos,* vol. 20, no. 8, pp. 2253-2425, Aug. 2010.

5. [Patent]

   H. Kim and L. O. Chua, **"Method of implementing memristor-based multilevel memory using reference resistor array,"** *United States Patent,* Jul. 2011.

   Filing number: US 13/009,969, Filing date: January 20, 2011
   Registered number: 8,416,604, Registered date: April 9, 2013

6. M. Itoh and L. O. Chua, "**Memristor hamiltonian circuits,"** *International journal of Bifurcation and Chaos,* vol. 21, no. 9, pp. 2395-2425, Sep. 2011.

7. H. Kim, M. P.Sah, C. Yang, T. Roska and L.O. Chua, **"Neural synaptic weighting with a pulse-based memristor circuit,"** *IEEE Tran. Circuits and Systems-I,* vol. 59, no. 1, pp.148-158, Jan. 2012.

8. H. Kim and S. P. Adhikari, **"Memistor is not memristor,"** *IEEE Circuits and Systems Magazine,* vol. 12, no. 1, pp. 75-78, Jan. 2012.

9. M. P. Sah, C. Yang, H. Kim and L.O. Chua, **"A voltage mode memristor bridge synaptic circuit with memristor emulators,"** *Sensors,* vol. 12, no. 3, pp. 3587-3604, Mar. 2012.

10. L. Chua, V. Sbitnev and H. Kim, "**Hodgkin–huxley axon is made of memristors,"** *International journal of Bifurcation and Chaos,* vol. 22, no. 3, pp. 123001(1)-123001(48), Mar. 2012.

11. L. Chua, V. Sbitnev and H. Kim, **"Neurons are poised near the edge of chaos,"** *International journal of Bifurcation and Chaos,* vol. 22, no. 4, pp. 1250098(1)-1250098(49), Apr. 2012.

12. H. Kim, M. P.Sah, C. Yang, T. Roska and L.O. Chua, **"Memristor bridge synapses,"** *Proc. of IEEE, Special issue on Memristors: Devices, Models and Applications,* vol. 100, no. 6, pp. 2061-2070, Jun. 2012.

13. L. Chua, **"The fourth element,"** *Proc. of IEEE, Special issue on Memristors: Devices, Models and Applications,* vol. 100, no. 6, pp. 1920-1927, Jun. 2012.

14. S. P. Adhikari, C. Yang, H. Kim and L. O. Chua, **"Memristor bridge synapse-based neural network and its learning,"** *IEEE Tran. Neural Networks and Learning Systems* vol. 23, no. 9, pp. 1426-1434, Sep. 2012

15. H. Kim, M. P. Sah, C. Yang, S. Cho and L. O. Chua, **"Memristor emulator for memristor circuit applications,"** *IEEE Tran. Circuits and Systems I,* vol. 59, no. 10, pp. 2422 - 2431, Oct. 2012.

16. S. P. Adhikari and H. Kim, **"Why are memristor and memistor different devices?,"** *IEEE Tran. Circuits and Systems I,* vol. 59, no. 11, pp. 2611-2618, Nov. 2012.

17**.** S. P. Adhikari, H. Kim, B. S. Kong and L. O. Chua**, "Memristance drift avoidance with charge bouncing for memristor-based nonvolatile memories",** *Journal of the Korean Physical Society*, Vol. 61, No. 9, pp. 1418-1421, Nov. 2012.

SUMMARY OF RESEARCH

Following are edited *abstracts* from the 17 published publications cited above.

1. RESISTANCE SWITCHING MEMORIES ARE MEMRISTORS

L. Chua

Abstract

All 2-terminal non-volatile memory devices based on *resistance switching* are *memristors*, regardless of the device material and physical operating mechanisms. They all exhibit a distinctive "fingerprint" characterized by a *pinched hysteresis loop* confined to the first and the third quadrants of the *v–i* plane whose contour shape in general changes with both the amplitude and frequency of any periodic "sinewave- like" input voltage source, or current source. In particular, the pinched hysteresis loop shrinks and tends to a straight line as frequency increases. Though numerous examples of voltage vs. current pinched hysteresis loops have been published in many unrelated fields, such as biology, chemistry, physics, etc., and observed from many unrelated phenomena, such as gas discharge arcs, mercury lamps, power conversion devices, earthquake conductance variations, etc., we restrict our examples in this *tutorial* to solid state and/or nano devices where copious examples of published pinched hysteresis loops abound. In particular, we sampled arbitrarily, one example from each year between the years 2000 and 2010, to demonstrate that the memristor is a device that does not depend on any particular material, or physical mechanism. For example, we have shown that *spin-transfer magnetic tunnel junctions* are examples of memristors. We have also demonstrated that both *bipolar* and *unipolar* resistance switching devices are memristors.

The goal of this *tutorial* is to introduce some fundamental circuit-theoretic concepts and properties of the memristor that are relevant to the analysis and design of *non-volatile* nano memories where binary bits are stored as resistances manifested by the memristor's continuum of equilibrium states. Simple pedagogical examples will be used to illustrate, clarify, and demystify various misconceptions among the uninitiated.

2. TOPOLOGICAL ANALYSIS OF CHAOTIC SOLUTION OF A THREE-ELEMENT MEMRISTIVE CIRCUIT

J. M. Ginoux, C. Letellier and L. Chua

Abstract

In classical electronics, there are three passive circuit elements: the resistor, the capacitor and the inductor. In 1971, Leon Chua introduced a fourth "missing" element which he named a memristor — for memory resistor — by using symmetry arguments. Chua also derived the properties of this element. However, it is only in 2008 that Strukov and co-workers found a memristance arising in a nanoscale system in which solid-state electronic and ionic transport are coupled under an external bias voltage. In 1976, Chua and Kang generalized the memristor to a broader class of nonlinear dynamical systems they called memristive systems.

Some chaotic memristive electronic circuits were already proposed but they were four-dimensional. It is only recently that a three-dimensional system was proposed to describe a memristive circuit. This is the simplest three-element electronic circuit producing chaotic behaviors since it is only made of two linear passive energy-storage elements, and an active memristive device. The system here studied has five linear terms and two nonlinear terms. The fact that this simple memristive circuit is not a minimal system is an advantage since very often, minimal systems have very tiny parameter domains associated with chaotic regimes and a small attraction basin. As a consequence, the simple memristive circuit has a quite large attraction basin and a quite large domain of its parameter space over which the system is chaotic.

In this paper, we present a topological analysis of chaotic attractors of this memristive circuit.

3. AUTOASSOCIATIVE MEMORY CELLULAR NEURAL NETWORKS

M. Itoh and L. Chua

Abstract

An autoassociative memory is a device which accepts an input pattern and generates an output as the stored pattern which is most closely associated with the input. In this paper, we propose an *autoassociative memory cellular neural network*, which consists of one-dimensional cells with spatial derivative inputs, thresholds and memories. Computer simulations show that it exhibits good performance in face recognition: The network can retrieve the whole from a part of a face image, and can reproduce a clear version of a face image from a noisy one. For human memory, research on "visual illusions" and on "brain damaged visual perception", such as the Thatcher illusion, the hemispatial neglect syndrome, the split-brain, and the hemispheric differences in recognition of faces, has fundamental importance. We simulate them in this paper using an autoassociative memory cellular neural network. Furthermore, we generate many composite face images with spurious patterns by applying genetic algorithms to this network. We also simulate a morphing between two faces using autoassociative memory.

4. A NONLINEAR DYNAMICS PERSPECTIVE OF WOLFRAM'S NEW KIND OF SCIENCE. PART XIV: MORE BERNOULLI σ_T -SHIFT RULES

L. Chua and G. Pazienza

Abstract

Over the past eight years, we have studied one of the simplest, yet extremely interesting, dynamical systems; namely, the one-dimensional binary Cellular Automata. The most remarkable results have been presented in a series of papers which is concluded by the present article. The final step of our odyssey is devoted to the analysis of the second half of the 30

Bernoulli σ_τ –shift rules, which constitute the largest among the six groups in which we classified the 256 local rules. For all these 15 rules, we present the basin-tree diagrams obtained by using each bit string with $L \leq 8$ as initial state, a summary of the characteristics of their ω-limit orbits, and the space-time patterns generated from the superstring. Also, in the last section we summarize the main results we obtained by means of our "nonlinear dynamics perspective".

5. **[PATENT]**

METHOD OF IMPLEMENTING MEMRISTOR-BASED MULTILEVEL MEMORY USING REFERENCE RESISTOR ARRAY

Filing number: US 13/009,969, Filing date: January 20, 2011
Registered number: 8,416,604, Registered date: April 9, 2013

H. Kim and L. O. Chua

Abstract

The present invention relates to a memristor, and more particularly, to a method of implementing a memristor-based multilevel memory using a reference resistor array and a write-in circuit and a read-out/restoration circuit for the memristor-based multilevel memory, in which a memristor can be used as a multilevel memory. In the present invention, a reference resistance value is written in a selected memristor of a memristor array by applying repeatedly current pulses of which widths are proportional to the difference between the resistances of the selected memristor and the selected node of the reference resistor array.

6. **MEMRISTOR HAMILTONIAN CIRCUITS**

M. Itoh and L. O. Chua

Abstract

We prove analytically that 2-element *memristive circuits* consisting of a *passive linear inductor* in parallel with a *passive memristor*, or an *active memristive device*, can be described explicitly by a *Hamiltonian* equation, whose solutions can be periodic or damped, and can be represented analytically by the constants of the motion along the circuit Hamiltonian. Generalizations to 3-element and 2N-element memristive Hamiltonian circuits are also presented where complex bifurcation phenomena including *chaos*, abound.

7. NEURAL SYNAPTIC WEIGHTING WITH A PULSE-BASED MEMRISTOR CIRCUIT

H. Kim, M. P.Sah, C. Yang, T. Roska and L.O. Chua

Abstract

A pulse-based programmable memristor circuit for implementing synaptic weights for artificial neural networks is proposed. In the memristor weighting circuit, both positive and negative multiplications are performed via a charge-dependent Ohm's law ($v=M(q)\times i$). The circuit is composed of five memristors with bridge-like connections and operates like an artificial synapse with pulse-based processing and adjustability. The sign switching pulses, weight setting pulses and synaptic processing pulses are applied through a shared input terminal. Simulations are done with both linear memristor and window-based nonlinear memristor models.

8. MEMISTOR IS NOT MEMRISTOR

H. Kim and S. P. Adhikari

Abstract

This note clarifies the circuit-theoretic differences between a memristor and a memistor.

9. A VOLTAGE MODE MEMRISTOR BRIDGE SYNAPTIC CIRCUIT WITH MEMRISTOR EMULATORS

M. P.Sah, C. Yang, H. Kim and L.O. Chua

Abstract

A memristor bridge neural circuit which is able to perform signed synaptic weighting was proposed in our previous study, where the synaptic operation was verified via software simulation of the mathematical model of the HP memristor. This study is an extension of the previous work advancing toward the circuit implementation where the architecture of the memristor bridge synapse is built with memristor emulator circuits. In addition, a simple neural network which performs both synaptic weighting and summation is built by combining memristor emulators-based synapses and differential amplifier circuits. The feasibility of the memristor bridge neural circuit is verified *via* SPICE simulations.

10. HODGKIN–HUXLEY AXON IS MADE OF MEMRISTORS

L. Chua, V. Sbitnev and H. Kim

Abstract

This paper presents a rigorous and comprehensive nonlinear circuit-theoretic foundation for the *memristive Hodgkin–Huxley Axon Circuit model*. We show that the Hodgkin–Huxley Axon comprises a *potassium ion-channel memristor* and a *sodium ion-channel memristor*, along with some mundane circuit elements. From this new perspective, many hitherto unresolved *anomalous* phenomena and paradoxes reported in the literature are explained and clarified. The

yet unknown nonlinear dynamical mechanisms which give birth to the *action potentials* remain hidden within the memristors, and the race is on for uncovering the ultimate truth.

11. **NEURONS ARE POISED NEAR THE EDGE OF CHAOS**

L. Chua, V. Sbitnev and H. Kim

Abstract

This paper shows the *action potential (spikes)* generated from the Hodgkin–Huxley equations emerges near the *edge of chaos* consisting of a tiny subset of the *locally active* regime of the HH equations. The main result proves that the eigenvalues of the 4 × 4 Jacobian matrix associated with the mathematically intractable system of four nonlinear differential equations are identical to the zeros of a *scalar complexity function* from complexity theory. Moreover, we show the loci of a pair of complex-conjugate zeros migrate continuously as a function of an externally applied DC current excitation emulating the net synaptic excitation current input to the neuron. In particular, the pair of complex-conjugate zeros move from a *subcritical* Hopf bifurcation point at low excitation current to a *super-critical* Hopf bifurcation point at high excitation current. The spikes are generated as the excitation current approaches the vicinity of the *edge of chaos*, which leads to the onset of the *subcritical* Hopf bifurcation regime. It follows from this in-depth qualitative analysis that *local activity is the origin of spikes.*

12. **MEMRISTOR BRIDGE SYNAPSES**

H. Kim, M. P.Sah, C. Yang, T. Roska and L.O. Chua

Abstract

In this paper, we propose a memristor bridge circuit consisting of four identical memristors that is able to perform zero, negative, and positive synaptic weightings. Together with three additional transistors, the memristor bridge weighting circuit is able to perform synaptic operation for neural cells. It is compact as both weighting and weight programming are performed in a memristor bridge synapse. It is power efficient, since the operation is based on

pulsed input signals. Its input terminals are utilized commonly for applying both weight programming and weight processing signals via time sharing. In this paper, features of the memristor bridge synapses are investigated using the TiO_2 memristor model via simulations.

13. **THE FOURTH ELEMENT**

L. Chua

Abstract

This tutorial clarifies the axiomatic definition of ($v^{(\alpha)}$; $i^{(\beta)}$) circuit elements via a lookup table dubbed an A-pad, of admissible (v; i) signals measured via Gedanken probing circuits. The ($v^{(\alpha)}$; $i^{(\beta)}$) elements are ordered via a complexity metric. Under this metric, the memristor emerges naturally as the fourth element, characterized by a state-dependent Ohm's law. A logical generalization to memristive devices reveals a common fingerprint consisting of a dense continuum of pinched hysteresis loops whose area decreases with the frequency ω and tends to a straight line as $\omega \sim \infty$, for all bipolar periodic signals and for all initial conditions. This common fingerprint suggests that the term memristor be used hence-forth as a moniker for memristive devices.

14. **MEMRISTOR BRIDGE SYNAPSE-BASED NEURAL NETWORK AND ITS LEARNING**

S. P. Adhikari, C. Yang, H. Kim and L. O. Chua

Abstract

Analog hardware architecture of a memristor bridge synapse-based multi-layer neural network and its learning scheme is proposed. The use of memristor bridge synapse in the proposed

architecture solves one of the major problems regarding non-volatile weight storage in analog neural network implementations. To compensate for the spatial non-uniformity and non-ideal response of the memristor bridge synapse, a software-assisted hardware modified chip-in-the-loop learning scheme suitable for the proposed neural network architecture is also proposed. In the proposed method, the initial learning is conducted in software and the behavior of the software-trained network is learned by the hardware network by learning each of the single layered neurons of the network independently. The forward calculation of the single-layered neuron learning is implemented on circuit hardware, and followed by a weight updating phase assisted by a host computer. Unlike conventional chip-in-the-loop learning, the need for the readout of synaptic weights for calculating weight updates in each epoch is eliminated by virtue of the memristor bridge synapse and the proposed learning scheme. The hardware architecture along with the successful implementation of software-assisted hardware proposed learning on a 3-bit parity network, and on a car detection network are also presented.

15. **MEMRISTOR EMULATOR FOR MEMRISTOR CIRCUIT APPLICATIONS**

H. Kim, M. P. Sah, C. Yang, S. Cho and L. O. Chua,

Abstract

A memristor emulator which imitates the behavior of a TiO_2 memristor is presented. Our emulator is built from off-the-shelf solid state components. To develop real world memristor circuit applications, the emulator can be used for breadboard experiments in real time. Two or more memristor emulators can be connected in serial, in parallel, or in hybrid (serial and parallel combined) with identical or opposite polarities. With a simple change of connection, each memristor emulator can be switched between a decremental configuration or an incremental configuration. The hardware and spice simulation of the proposed emulator showed promising results that provides an alternative solution of *hp* TiO_2 memristor model in real circuit.

16. **WHY ARE MEMRISTOR AND MEMISTOR DIFFERENT DEVICES?**

S. P. Adhikari and H. Kim

Abstract

This paper presents a circuit-theoretic foundation of the "memristor," and clarifies why it is fundamentally different from a 3-terminal device with a similarly-sounding name called the "memistor." Here we show that while the memristor is a basic 2-terminal circuit element based on classic nonlinear circuit theory, the memistor is an ad hoc 3-terminal gadget devised for one specific application, and does not qualify as a 3-terminal circuit element because it is impossible to predict its behavior when connected with other circuit elements.

17. **MEMRISTANCE DRIFT AVOIDANCE WITH CHARGE BOUNCING FOR MEMRISTOR-BASED NONVOLATILE MEMORIES**

S. P. Adhikari, H. Kim, B. S. Kong and L. O. Chua

Abstract

A charge bouncing solution to avoid the undesirable drift in the programmed memory during readout of memristor-based non-volatile memory is proposed. Memristor memory can be programmed by strong programming signals, and the programmed memristance can be readout by weak readout signals. Though readout signals are weak compared to programming signals, readout charge is accumulated over time and leads to an undesirable drift of the operating point. This causes error in the programmed memory. Memristance drift is an important problem for practical utilization of memristors as memory. The only way presented so far to avoid drift is by converting input signals to doublets but non-ideal doublet signals still cause drifting problem. In the proposed method, drift is avoided with a capacitor in such a way that all the charge injected to the memristor during readout is stored in a capacitor, and bounced back through the memristor after completing the readout. Experimental results showing an excellent recovery from the

temporal memristance drift using singlet pulses rather than the conventionally used doublet pulses for memristive memory readout are also presented.